MOTENC-100

MOTENC-100
8-Axis PCI Motion & I/O Control Board

Reference Manual
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1. Overview

The MOTENC-100 board is a passive motion control board with a 3.3 and 5 Volts tolerant PCI bus interface. The card has several devices on board that are required for motion control applications, e.g., Encoder counters, DACs, ADCs, and I/Os. All devices are under direct control of host PC. Following is a list of features available on board:

Analog Inputs: Range +/-5Volts, 14-bit Resolution. 8-Channels
Analog Outputs: +/-10V, 13-Bit Resolution, 8-Channels
Encoders: 8 Differential Encoder Inputs. 32-Bit Resolution
I/Os: 100 Digital I/O (68 Inputs & 32 Outputs) in four 50-pin headers. (Opto-22 compatible)
+5V available on headers, Fused (Resetable), MAX current 2A
Programmable Timer Interrupts
Watch Dog Timer
Hardware ESTOPs (Jumpers on board to override if not needed)
Filters at Digital Inputs remove High frequency noise
Hardware Board ID for multiple board applications
EMC ready

The MOTENC-100 board incorporates a 32-bit data bus, and requires all read & write access to be 32-bit wide. The board is memory mapped (no I/O mapping) and takes up 512 bytes of address space in PCI region (BAR) number 2. The Read/Write Access must also be Double Word (32bit) aligned.

Important: All offsets and Indexes in this document are zero based. All numbers are decimal unless stated as Hex by using the “C” 0x notation.

2. Memory Register Map

Register Offset	Description
0 (Byte Offset 0)	**Read:** Provides the signed 32-bit Counter Data for Encoder 0 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 0. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 5 bit 24. The current level of the Index line is available at offset 5 bit 20. Upon latching of the Index Pulse, the corresponding Encoder Counter is reset to zero.
1 (Byte Offset 4)	**Read:** Provides the signed 32-bit Counter Data for Encoder 1 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 1. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 5 bit 25. The current level of the Index line is available at offset 5 bit 21. Upon latching of the Index Pulse, the corresponding Encoder Counter is reset to zero.
2 (Byte Offset 8)	**Read:** Provides the signed 32-bit Counter Data for Encoder 2 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 2. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 5 bit 26. The current level of the Index line is available at offset 5 bit 22. Upon latching of Index pulse, the corresponding Encoder Counter is reset to zero.
3 (Byte Offset 12)	**Read:** Provides the signed 32-bit Counter Data for Encoder 3 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 3. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 5 bit 27. The current level of the Index line is available at offset 5 bit 23. Upon latching of Index pulse, the corresponding Encoder Counter is reset to zero.

Register Offset	Bit(s)	Description
4 (Byte Offset 16) Bit 0...15 = Read & Write Bit 16...31 = Read Only	**Read**	
	0 … 15	Read Outputs number 0 thru 15
	16	Input 0 (Limit High for Axis 0)
	17	Input 1 (Limit Low for Axis 0)
	18	Input 2 (Home for Axis 0)
	19	Input 3 (Amp Fault for Axis 0)
	20	Input 4 (Limit High for Axis 1)
	21	Input 5 (Limit Low for Axis 1)
	22	Input 6 (Home for Axis 1)
	23	Input 7 (Amp Fault for Axis 1)
	24	Input 8 (Limit High for Axis 2)
	25	Input 9 (Limit Low for Axis 2)
	26	Input 10 (Home for Axis 2)
	27	Input 11 (Amp Fault for Axis 2)
	28	Input 12 (Limit High for Axis 3)
	29	Input 13 (Limit Low for Axis 3)
	30	Input 14 (Home for Axis 3)
	31	Input 15 (Amp Fault for Axis 3)
	Write	
	0 … 15	Write Outputs number 0 thru 15
5 (Byte Offset 20) Bit 0...3 = Read & Write Bit 4...31 = Read Only	**Read**	
	0 … 15	Inputs 16 … 31
	16	Jumper J3 Board ID 0 state (Installed = 0)
	17	Jumper J3 Board ID 1 state (Installed = 0)
	18	ADC_DONE bit From Analog-To-Digital Converter (Active Low)
	19	ESTOP State. (Active High)
	20 … 23	Index Level for Encoder 0 … 3
	24 … 27	Index Latch Flag for Encoder 0 … 3 (Active High)
	28 … 30	Reserved
	31	Reserved
	Write	
	0...3	Writing a 1 to these bits resets the Encoder Counter 0…3, e.g., writing 0xF (1111 binary) will reset counters 0 through 3, writing 0x2 (0010 binary) resets only encoder counter 1, and so on.

Register Offset	Description
6 (Byte Offset 24)	Reserved
7 (Byte Offset 28)	Reserved

Register Offset	Description
8 (Byte Offset 32)	**Read:** Provides the signed 32-bit Counter Data for Encoder 4 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 4. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 13 bit 24. The current level of the Index line is available at offset 13 bit 20. Upon latching of the Index Pulse, the corresponding Encoder Counter is reset to zero.
9 (Byte Offset 36)	**Read:** Provides the signed 32-bit Counter Data for Encoder 5 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 5. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 13 bit 25. The current level of the Index line is available at offset 13 bit 21. Upon latching of the Index Pulse, the corresponding Encoder Counter is reset to zero.
10 (Byte Offset 40)	**Read:** Provides the signed 32-bit Counter Data for Encoder 6 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 6. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 13 bit 26. The current level of the Index line is available at offset 13 bit 22. Upon latching of Index pulse, the corresponding Encoder Counter is reset to zero.
11 (Byte Offset 44)	**Read:** Provides the signed 32-bit Counter Data for Encoder 7 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 7. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 13 bit 27. The current level of the Index line is available at offset 13 bit 23. Upon latching of Index pulse, the corresponding Encoder Counter is reset to zero.

Register Offset	Bit(s)	Description
12 (Byte Offset 48) Bit 0...15 = Read & Write Bit 16...31 = Read Only	**Read**	
	0 … 15	Read Outputs number 16 thru 31
	16	Input 32 (Limit High for Axis 4)
	17	Input 33 (Limit Low for Axis 4)
	18	Input 34 (Home for Axis 4)
	19	Input 35 (Amp Fault for Axis 4)
	20	Input 36 (Limit High for Axis 5)
	21	Input 37 (Limit Low for Axis 5)
	22	Input 38 (Home for Axis 5)
	23	Input 39 (Amp Fault for Axis 5)
	24	Input 40 (Limit High for Axis 6)
	25	Input 41 (Limit Low for Axis 6)
	26	Input 42 (Home for Axis 6)
	27	Input 43 (Amp Fault for Axis 6)
	28	Input 44 (Limit High for Axis 7)
	29	Input 45 (Limit Low for Axis 7)
	30	Input 46 (Home for Axis 7)
	31	Input 47 (Amp Fault for Axis 7)
	Write	
	0 … 15	Write Outputs number 16 thru 31
13 (Byte Offset 52) Bit 0...3 = Read & Write Bit 4...31 = Read Only	**Read**	
	0 … 19	Inputs 48 … 67
	20 … 23	Index Level for Encoder 4 … 7
	24 … 27	Index Latch Flag for Encoder 4 … 7 (Active High)
	28 … 30	Reserved
	31	Reserved
	Write	
	0...3	Writing a 1 to these bits resets the Encoder Counter 4…7, e.g., writing 0xF (1111 binary) will reset counters 4 through 7, writing 0x2 (0010 binary) resets only encoder counter 5, and so on.

Register Offset	Description
14 (Byte Offset 56)	Reserved
15 (Byte Offset 60)	Reserved

Register Offset	Description	
16 (Byte Offset 64) Write Only	Timer Compare Data for Programmable Timer Interrupts. Bits 0…7 are significant, bits 8…31 are don't care. Each Count Generates a delay of 15.5 micro-second. For example, to setup the timer for 1 mili-second cycle time, write a value of 64 (1000/15.5).	
17 (Byte Offset 68) Write Only	Writing a value of 1 clears and disables the programmable timer interrupt.	
18 (Byte Offset 72) Write Only	Writing a value of 1 enables the programmable timer interrupt cycle (one-shot) and the timer starts counting up. When the timer reaches the programmed value, it generates the timer interrupt. The ISR must clear the interrupt by writing at offset 17. After ISR finish work, it can restart the next timer cycle by writing to this register (offset 18).	
19 (Byte Offset 76) Write Only	**Bit(s)**	**Description**
	0	Watch Dog Time-Base Select. Writing a 0 selects the 8 mili-second time base. Writing a 1 selects the 16 mili-second time base.
	1	Reserved
	2	Watch Dog Enable Bit. Writing a 1 enables the Watch Dog circuit. Writing a 0 disables it.
	3	Reserved
	4	Enable watchdog reset when writing to DACs. Resetting the watchdog by writing to the DACs can be achieved by writing a 1 to this bit. This turns on the circuit that resets the watch-dog timer every time the DACs are written to. If this bit is reset (Default on power up), only writing to location 20 resets the watch-dog timer.

Register Offset	Description
20 (Byte Offset 80) Write Only	Reset watchdog Timer. When WD is enabled, it must be reset within the selected 8 or 16 mili-sec time interval. Writing a value of 0x5A at this location resets the timer. If bit 4 at location 19 is set to 1, writing to any DAC also resets the WD timer.
21 … 23	Reserved
24 … 31 (Byte Offset 96…124) Write Only	DAC Channel 0…7 Data Write. Bits 0...12 are significant. **Transfer Function** **0x00000000 => +10 Volts** **0x00001000 => 0 Volts** **0x00001FFF => -10 Volts**
32 (Byte Offset 128) Read/Write	ADC - Analog to Digital Converter Data/Command read/write Register. Reading this location provides the conversion results (signed, 14 bits) of the ADC. Bits 0 though 13 are significant. When writing command, 4 LSBs (bits 0 thru 3) are used; the rest of the bits must be zero. Please review section 3 for more details.
33 … 39	Reserved
40 (Byte Offset 160) Write Only	Writing a 1 at this location initiates a conversion sequence.

3. Analog to Digital Converter – ADC Operation

The ADC used in MOTENC-100 board is MAXIMs MAX125.

Inputs:	8 Channels (2 groups of four inputs)
Resolution:	14 bits
Digital Output Range:	-8192 to +8191
Input voltage range:	-5Volts to +5Volts
Transfer function	0.61 mili-volt / 1 LSB.
Input current:	700 uA / Channel.

The MAX125 ADC has 8 Analog Inputs. The Inputs are configured as two banks of 4 inputs each. The header J5 connects to bank A and J8 to bank B. On Power up or ESTOP, the device defaults to single channel conversion of bank A. The device can be programmed to convert 1, 2, 3 or 4 channels of the selected bank per sample. ADC_DONE (Loc 5 bit 18) goes Low when all channels are digitized.

The following table lists the command words. The commands are written to the ADC through location 32.

Command	Description
0	Analog Input 0 Conversion (J5)
1	Analog Inputs 0 and 1 Conversion (J5)
2	Analog Inputs 0,1, and 2 Conversion (J5)
3	Analog Inputs 0,1,2, and 3 Conversion (J5)
4	Analog Input 4 Conversion (J8)
5	Analog Inputs 4 and 5 Conversion (J8)
6	Analog Inputs 4,5, and 6 Conversion (J8)
7	Analog Inputs 4,5,6 and 7 Conversion (J8)
8	Power Down mode.

Starting a Conversion

After configuring the MAX125 with the appropriate command, write a 1 to location 40 to initiate a conversion sequence. The analog inputs are sampled. Do not start a new conversion while the conversion is in progress. Monitor the ADC_DONE bit. A Low level indicates the end of a conversion sequence.

Reading a Conversion

Digitized data from up to four channels are stored in the device internal memory. After reading the ADC_DONE signal in Low state, the user can access up to four conversion results by performing up to four read operations at location 32 sequentially. The first read also brings the ADC_DONE signal back to high level. The number of reads must match the programmed number of channel conversions. Multiple channel digitized-data must be read sequentially.

4. Digital To Analog Converter – DAC Operation

The DAC used in MOTENC-100 board is MAXIMs MAX547.

Number of Outputs:	8 Channels
Conversion Time	5 microsecond per channel
Resolution	13bit
Data Range	0x0000 to 0x1FFF (0 to 8191)
Transfer Function	Vout = –10 x ((Data / 4096) – 1)
	0x0000 ≈ +10 V
	0x1000 ≈ 0 V
	0x1FFF ≈ -10 V

Data is written sequentially for all eight channels from location 24 thru 31 corresponding to channel 0 thru 7. The channel data is written to the DAC by a single write cycle, therefore, updating all eight channels will require eight write cycles.

5. E-STOP Operation & Jumper Settings

The Jumper J3 is used for ESTOP and Board ID configuration. The board has three ESTOP signals, two on ENCTERM breakout board terminal J22, and one on the PCI board terminal J4. Activating any ESTOP signal will reset the board. Installing Jumpers on J3 ESP1, ESP2 and ESP3 can individually disable each ESTOP signal. Installing Jumper at J3 ALL disables the entire ESTOP circuit.

When any of the ESTOP input is activated (Active Low), the board goes into a reset state as long as the ESTOP pin is active. In the reset state, all DAC outputs are set to zero volt, all digital outputs are set to off state, and encoder counters are set to zero.

6. Board Headers and Terminals

The header J5 and J8 connects to the ENCTERM breakout board headers J1 and J2 respectively. These headers provide signals for Encoder, DAC, ADC, and ESTOP.

Header J6, J7, J9 and J10 provides digital I/O connections. These headers are opto-22 compatible. Each header provides 16 inputs and 8 outputs (Digital). There is no optical isolation on the PCI board itself. The breakout board (IOTERM) or the Opto-22 type Digital I/O board provides optical isolation.

The Screw Terminal J4 on the PCI board provides connections for 5 Volts, Ground, watchdog output, ESTOP #3 input, and inputs 64 thru 67. These signals are TTL compatible and should never be used with any voltage higher than 5 volts.

The watchdog output is Active low. If the PC software enables the watchdog circuit and fails to reset the watchdog timer within the configured amount of time, the watchdog circuit resets the entire board and sets the watchdog output to logic 0. All DAC outputs, Digital outputs and Encoder counter are reset to zero. The watchdog output pin can be used to monitor this state by an external controller if needed.

The ESTOP terminal on J4 is active low, i.e., switching it to ground activates it.

The Inputs 64 thru 67 on terminal J4 are active Low.

All signals of terminal J4 are NOT opto-isolated, therefore take proper measures when wiring with external power supplies.

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