MOTENC-Lite

MOTENC-Lite
4-Axis PCI Motion & I/O Control Board

Reference Manual
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1. Overview

The ***MOTENC-Lite*** board is a passive motion control board with a 3.3 and 5 Volts tolerant PCI bus interface. The card has several devices on board that are required for motion control applications, e.g., Encoder counters, DACs, ADCs, and I/Os. All devices are under direct control of host PC. Following is a list of features available on board:

Analog Inputs: Range +/-5Volts, 14-bit Resolution. 8-Channels
Analog Outputs: +/-10V, 13-Bit Resolution, 8-Channels
Encoders: Differential Encoder Inputs. 32-Bit Resolution, 4-Channels
I/Os: 32 Inputs & 16 Outputs in two 50-pin headers. (Opto-22 compatible)
Additional 6 inputs and 4 outputs on SIP headers.
Programmable Timer Interrupts
Watch Dog Timer
Hardware Board ID for multiple board applications(optional)

The ***MOTENC-Lite*** board incorporates a 32-bit data bus, and requires all read & write access to be 32-bit wide. The board is memory mapped (no I/O mapping) and takes up 512 bytes of address space in PCI region (BAR) number 2. The Read/Write Access must be Double Word (32bit) aligned.

Important: All register Indexes and bit offsets in this document are zero based. Pin numbers are 1 based. All numbers are decimal unless stated as Hex by using the “C” 0x notation.

2. Memory Register Map

Register Offset	Description
0 (Byte Offset 0)	**Read:** Provides the signed 32-bit Counter Data for Encoder 0 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 0. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 5 bit 24. The current level of the Index line is available at offset 5 bit 20. Upon latching of Index Pulse, the corresponding Encoder Counter is reset to zero. (see below)
1 (Byte Offset 4)	**Read:** Provides the signed 32-bit Counter Data for Encoder 1 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 1. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 5 bit 25. The current level of the Index line is available at offset 5 bit 21. Upon latching of Index Pulse, the corresponding Encoder Counter is reset to zero.
2 (Byte Offset 8)	**Read:** Provides the signed 32-bit Counter Data for Encoder 2 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 2. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 5 bit 26. The current level of the Index line is available at offset 5 bit 22. Upon latching of Index pulse, the corresponding Encoder Counter is reset to zero.
3 (Byte Offset 12)	**Read:** Provides the signed 32-bit Counter Data for Encoder 3 **Write:** Writing a 1 at this location turns on the latching of Index Pulse for Encoder 3. Writing a Zero will reset this latch. The current state of the Index Flag can be read at offset 5 bit 27. The current level of the Index line is available at offset 5 bit 23. Upon latching of Index pulse, the corresponding Encoder Counter is reset to zero.

Auto Homing Latch Circuit

The Index pulse latch is used to reset the counter on the next index pulse to auto-home the axis. To enable this circuit, write a 1 to Register locations 0 .. 3 for encoder 0 .. 3 respectively. There are 4 latches, one for each encoder, work independently of each other. The software can watch the state (flag) of latches at bit 24 .. 27 of register location 5 for encoder 0 .. 3 respectively. When the flag is set, this indicates that the hardware has reset the counters on the detection of index pulse. The software can write 0 to register location 0..3 to clear the flags for the encoder (optional).

Register Offset	Bit(s)	Description
4 (Byte Offset 16) Bit 0...15 = Read & Write Bit 16...31 = Read Only	**Read**	
	0 … 15	Read Outputs 0 thru 15 (verify)
	16 … 31	Read Inputs 0…15 (Land On J5)
	Write	
	0 … 15	Write Outputs 0 thru 15 (Land On J5 and J4)
	16…31	No write operation (these bits are read only)
5 (Byte Offset 20) Bit 0...3 = Read & Write Bit 4...31 = Read Only	**Read**	
	0 … 15	Inputs 16 … 31 (Land On J4)
	16	Jumper J7 Board ID 0 state (Installed = 0)
	17	Jumper J7 Board ID 1 state (Installed = 0)
	18	ADC_DONE bit From Analog-To-Digital Converter (Active Low)
	19	Reserved
	20 … 23	Index Level for Encoder 0 … 3
	24 … 27	Index Latch Flag for Encoder 0 … 3 (Active High)
	28 … 30	Reserved
	31	Reserved
	Write	
	0...3	Writing a 1 to these bits resets the Encoder Counter 0…3, e.g., writing 0xF (1111 binary) will reset counters 0 through 3, writing 0x2 (0010 binary) resets only encoder counter 1, and so on.

Register Offset	Bit(s)	Description
6 (Byte Offset 24)	**Read**	
	0…3	Outputs 16…19 (Verify) (Land on J8 pin2..5)
	8	Encoder 0 Level A
	9	Encoder 0 Level B
	10	Encoder 1 Level A
	11	Encoder 1 Level B
	12	Encoder 2 Level A
	13	Encoder 2 Level B
	14	Encoder 3 Level A
	15	Encoder 3 Level B
	16..21	Inputs 32…37 (Land on J6)
	22	Watchdog state
	23	Jumper State J7.1 (Installed = 0)
	Write	
	0…3	Outputs 16…19 (Land on J8 pin2..5)
7 (Byte Offset 28) READ Only	**Reads value of 1 to indicate this is *MOTENC-Lite* Board. For Motenc-100, this location will always read 0.**	

Register Offset	Description
8 .. 15 (Byte Offset 32..60)	Reserved

<table>
<tr><th>Register Offset</th><th colspan="2">Description</th></tr>
<tr><td>16
(Byte Offset 64)
Write Only</td><td colspan="2">Timer Compare Data for Programmable Timer Interrupts. Bits 0…7 are significant, bits 8…31 are don't care. Each Count Generates a delay of 15.5 micro-second. For example, to setup the timer for 1 mili-second cycle time, write a value of 64 (1000/15.5).</td></tr>
<tr><td>17
(Byte Offset 68)
Write Only</td><td colspan="2">Writing a value of 1 clears and disables the programmable timer interrupt.</td></tr>
<tr><td>18
(Byte Offset 72)
Write Only</td><td colspan="2">Writing a value of 1 enables the programmable timer interrupt cycle (one-shot) and the timer starts counting up. When the timer reaches the programmed value, it generates the timer interrupt. The ISR must clear the interrupt by writing at offset 17. After ISR finish work, it can restart the next timer cycle by writing to this register (offset 18).</td></tr>
<tr><td rowspan="6">19
(Byte Offset 76)
Write Only</td><td>Bit(s)</td><td>Description</td></tr>
<tr><td>0</td><td>Watch Dog Time-Base Select.
Writing a 0 selects the 8 mili-second time base. Writing a 1 selects the 16 mili-second time base.</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>2</td><td>Watch Dog Enable Bit. Writing a 1 enables the Watch Dog circuit. Writing a 0 disables it.</td></tr>
<tr><td>3</td><td>Reserved</td></tr>
<tr><td>4</td><td>Enable watchdog reset when writing to DACs. Resetting the watchdog by writing to the DACs can be achieved by writing a 1 to this bit. This turns on the circuit that resets the watch-dog timer every time the DACs are written to. If this bit is reset (Default on power up), only writing to location 20 resets the watch-dog timer.</td></tr>
</table>

Register Offset	Description
20 (Byte Offset 80) Write Only	Reset watchdog Timer. When WD is enabled, it must be reset within the selected 8 or 16 mili-sec time interval. Writing a value of 0x5A at this location resets the timer. If bit 4 at location 19 is set to 1, writing to any DAC also resets the WD timer.
21 … 23	Reserved
24 … 31 (Byte Offset 96…124) Write Only	DAC Channel 0…7 Data Write. Bits 0...12 are significant. **Transfer Function** **0x00000000 => +10 Volts** **0x00001000 => 0 Volts** **0x00001FFF => -10 Volts**
32 (Byte Offset 128) Read/Write	ADC - Analog to Digital Converter Data/Command read/write Register. Reading this location provides the conversion results (signed, 14 bits) of the ADC. Bits 0 though 13 are significant. When writing command, 4 LSBs (bits 0 thru 3) are used; the rest of the bits must be zero. Please review section 3 for more details.
33 … 39	Reserved
40 (Byte Offset 160) Write Only	Writing a 1 at this location initiates a conversion sequence.

3. Analog to Digital Converter – ADC Operation

The ADC used in ***MOTENC-Lite*** board is MAXIMs MAX125.

Inputs:	8 Channels (2 groups of four inputs)
Resolution:	14 bits
Digital Output Range:	-8192 to +8191
Input voltage range:	-5Volts to +5Volts
Transfer function	0.61 mili-volt / 1 LSB.
Input current:	10 uA / Channel.

The MAX125 ADC has 8 Analog Inputs. The Inputs are configured as two banks of 4 inputs each. The header J3 connects to both bank A and B. On Power up, the device defaults to single channel conversion of bank A. The device can be programmed to convert 1, 2, 3 or 4 channels of the selected bank per sample. ADC_DONE (Loc 5 bit 18) goes Low when all channels are digitized.

The following table lists the command words. The commands are written to the ADC through location 32.

Command	Description
0	Analog Input 0 Conversion
1	Analog Inputs 0 and 1 Conversion
2	Analog Inputs 0,1, and 2 Conversion
3	Analog Inputs 0,1,2, and 3 Conversion
4	Analog Input 4 Conversion
5	Analog Inputs 4 and 5 Conversion
6	Analog Inputs 4,5, and 6 Conversion
7	Analog Inputs 4,5,6 and 7 Conversion
8	Power Down mode.

Starting a Conversion

After configuring the MAX125 with the appropriate command, write a 1 to location 40 to initiate a conversion sequence. The analog inputs are sampled. Do not start a new conversion while the conversion is in progress. Monitor the ADC_DONE bit. A Low level indicates the end of a conversion sequence, i.e., conversion complete.

Reading a Conversion

Digitized data from up to four channels are stored in the device internal memory. After reading the ADC_DONE signal in Low state, the user can access up to four conversion results by performing up to four read operations at location 32 sequentially. The first read also brings the ADC_DONE signal back to high level. The number of reads must match the programmed number of channel conversions. Multiple channel digitized-data must be read sequentially.

4. Digital To Analog Converter – DAC Operation

The DAC used in ***MOTENC-Lite*** board is MAXIMs MAX547.

Number of Outputs:	8 Channels
Conversion Time	5 microsecond per channel
Resolution	13bit
Data Range	0x0000 to 0x1FFF (0 to 8191)
Transfer Function	Vout = –10 x ((Data / 4096) – 1)
	0x0000 ≈ +10 V
	0x1000 ≈ 0 V
	0x1FFF ≈ -10 V

Data is written sequentially for all eight channels from location 24 thru 31 corresponding to channel 0 thru 7. The channel data is written to the DAC by a single write cycle, therefore, updating all eight channels will require eight write cycles.

5. Board Headers Pin Assignments

Encoder and Analog Header

The 50pin header J3 provide signals for Encoder, DAC, and ADC. The 50pin ribbon connects to the breakout board pn 7525 which labels all signal names. Please refer to the board pn 7525 for signal assignments.

Digital I/O – Opto-22 Headers

Headers J5 and J4 provides digital I/O connections. These headers are opto-22 compatible. Each header provides 16 inputs and 8 outputs (Digital). There is no optical isolation on the PCI board itself. The breakout board (IOTERM pn 7535) or the Opto-22 type Digital I/O board provides optical isolation.

J5 Pin Assignments

Input #	Pin #		Input #	Pin #		Input #	Pin #		Input #	Pin #
0	1		4	9		8	17		12	25
1	3		5	11		9	19		13	27
2	5		6	13		10	21		14	29
3	7		7	15		11	23		15	31

Output #	Pin #		Output #	Pin #
0	33		4	41
1	35		5	43
2	37		6	45
3	39		7	47

All even numbered pins are tied to ground. Pin 49 in tied to +5 Volts.

J4 Pin Assignments

Input #	Pin #		Input #	Pin #		Input #	Pin #		Input #	Pin #
16	1		20	9		24	17		28	25
17	3		21	11		25	19		29	27
18	5		22	13		26	21		30	29
19	7		23	15		27	23		31	31

Output #	Pin #		Output #	Pin #
8	33		12	41
9	35		13	43
10	37		14	45
11	39		15	47

All even numbered pins are tied to ground. Pin 49 in tied to +5 Volts.

WatchDog Output Pin
The watchdog output is Active low. If the PC software enables the watchdog circuit and fails to reset the watchdog timer within the configured amount of time, the watchdog circuit resets the entire board and sets the watchdog output to logic 0. All DAC outputs, Digital outputs and Encoder counter are reset to zero. The watchdog output pin can be used to monitor this state by an external controller if needed. This pin is available on Header J8 pin 1. Software can also read the state of this pin at register location 6 bit 22.

Header J7:
Pin 1: Reserved
Pin 3: Board ID 0
Pin 5: Board ID 1

Pins 2,4, and 6 are tied to Ground.

Header J6:
Pin 1 … 6: Inputs 32 … 37
Pin 7: Reserved

Header J8:
Pin 1: Watchdog Output
Pin 2 … 5: Outputs 16 … 19

All signals on PCI board headers (J4, J5, J6, J7 and J8) are TTL level with NO Optical isolation, therefore, proper care must be taken when wiring these signals with external circuits. These signals are TTL compatible and should never be used with any voltage higher than 5 volts.

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